

1     1.     A circuit comprising:  
2             a first edge-to-pulse converter having a first input to receive an initiating signal  
3             and a second input to receive a terminating signal, the first edge-to-pulse converter to  
4             provide an intermediate initiating signal at an output; and  
5             a second edge-to-pulse converter having a first input to receive the intermediate  
6             initiating signal and a second input to receive the terminating signal, the second edge-to-  
7             pulse converter to provide a pulse having a width determined by a first edge of the  
8             intermediate initiating signal and a first edge of the terminating signal.

1     2.     The circuit of claim 1, wherein each of the first and second converters performs an AND  
2     operation on the signals applied to its first and second inputs.

1     3.     The circuit of claim 2, wherein the AND operation is performed by first and second  
2     transistors coupled in series and having a first conductivity type, the gates of the first and second  
3     transistors forming the first and second inputs of the converters.

1     4.     The circuit of claim 3, wherein each of the first and second converters further includes a  
2     pre-charge transistor coupled in series with the first and second transistors, a gate of the pre-  
3     charge transistor being coupled to the second input of its respective converter.

1 5. The circuit of claim 4, wherein the initiating and terminating signals are start and stop  
2 pulses, respectively, and the width of the intermediate initiating signal is determined by edges of  
3 the start and stop pulses.

1 6. The circuit of claim 1, wherein a trailing edge of the intermediate initiating signal is  
2 determined by a leading edge of the stop pulse.

1 7. The circuit of claim 1, wherein the first converter includes first, second and third  
2 transistors coupled in series between first and second reference voltages and an inverter coupled  
3 to a drain of the first transistor and the converter output.

1 8. The circuit of claim 7, wherein the first input is coupled to a gate of the second transistor  
2 and the second input is coupled to gates of the first and third transistors.

1 9. A method comprising:

2 initiating an intermediate signal responsive to detection of an initiating signal;

3 terminating the intermediate signal, responsive to detection of a terminating  
4 signal;

5 initiating an output signal, responsive to detection of the intermediate signal; and

6 terminating the output signal, responsive to detection of the terminating signal.

1 10. The method of claim 9, wherein initiating the intermediate signal comprises initiating the  
2 intermediate signal responsive to a leading edge of the initiating signal.

1 11. The method of claim 9, wherein terminating the intermediate signal comprises  
2 terminating the intermediate signal responsive to a leading edge of the terminating signal.

1 12. The method of claim 11, further comprising generating the terminating signal a selected  
2 interval following the initiating signal, the selected interval corresponding to a desired width of  
3 the output signal.

1 13. A circuit comprising:  
2 a start pulse source to generate a start pulse having a width;  
3 a stop pulse source to generate a stop pulse having a delay relative to the start  
4 pulse, determined by a bit;  
5 a first edge-to-pulse converter to generate an intermediate pulse having a width  
6 determined by the start pulse and a first edge of the stop pulse; and  
7 a second edge-to-pulse converter to generate a symbol having a width determined  
8 by a first edge of the intermediate pulse and the first edge of the stop pulse

1 14. The circuit of claim 13, wherein the first edge-to-pulse converter includes an AND gate  
2 that is driven by the start and stop pulses.

1 15. The circuit of claim 14, wherein the second edge-to-pulse converter includes an AND  
2 gate that is driven by the intermediate and stop pulses.

1 16. The circuit of claim 13, wherein the stop pulse source includes a sequence of delay  
2 modules that may be sampled at selected locations of the sequence to provide the selected delay.

1 17. A method comprising:  
2 initiating an intermediate signal, responsive to a first programming signal;  
3 initiating an output signal, responsive to the intermediate signal;  
4 terminating the output signal, responsive to a second programming signal; and  
5 terminating the intermediate signal, responsive to an event associated with the  
6 second programming signal.

1 18. The method of claim 17, wherein terminating the intermediate signal comprises:  
2 detecting a leading edge of the second programming signal; and  
3 terminating the intermediate signal responsive to detecting the leading edge of the  
4 second programming signal.

1 19. The method of claim 17, wherein terminating the intermediate signal comprises:  
2 detecting a trailing edge of the output signal; and  
3 terminating the intermediate signal responsive to detecting the trailing edge of the  
4 output signal.

1 20. The method of claim 17, wherein the event associated with the second programming  
2 signal is expiration of an interval that exceeds a delay between the first programming signal and  
3 a latest second programming signal, and terminating the intermediate signal comprises  
4 terminating the intermediate signal responsive to expiration of the interval.

1 21. The method of claim 17, wherein the event associated with the second programming  
2 signal is expiration of an interval that is less than a delay between the first programming signal  
3 and an earliest second programming signal, and terminating the intermediate signal comprises  
4 terminating the intermediate signal responsive to expiration of the interval.

1 22. A circuit comprising:  
2 a first module having first input to receive a first programming signal, a second  
3 input to receive a terminate signal, the first module to initiate an intermediate signal  
4 responsive to the first programming signal and to terminate the intermediate signal  
5 responsive to the terminate signal; and

6                   a second module having a first input to receive the intermediate signal and a  
7                   second input to receive a second programming signal, the second module to initiate and  
8                   terminate an output signal, responsive to the intermediate signal and the second  
9                   programming signal, respectively, wherein the terminate signal for the first module is  
10                  related to the second programming signal.

1   23.    The circuit of claim 22, wherein the terminate signal for the first module is the second  
2   programming signal.

1   24.    The circuit of claim 23, wherein the first module terminates the intermediate signal  
2   responsive to a leading edge of the second programming signal.

1   25.    The circuit of claim 22, wherein the terminate signal for the first module is related to the  
2   output signal.

1   26.    The circuit of claim 25, wherein the first module terminates the intermediate signal  
2   responsive to a trailing edge of the output signal.

1